

CLAIMS

WHAT IS CLAIMED IS:

1. A CDMA demodulator, comprising:
 - 2 a finger timing unit for generating signals indicating cycle boundaries for a plurality of fingers; and
 - 4 an offline processing unit for receiving and storing samples and processing symbols from the stored samples for the plurality of fingers in response to the cycle
 - 6 boundary signals.
2. The demodulator of claim 1, further comprising a digital signal processor (DSP)
 - 2 for symbol demodulating and combining the processed symbols corresponding to the plurality of fingers.
3. The demodulator of claim 1, further comprising an engine for symbol
 - 2 demodulating and combining high rate symbols corresponding to the plurality of fingers.
4. A CDMA demodulator, comprising:
 - 2 a memory for storing samples according to a memory address;
 - a finger timing unit for producing a time reference for each of a plurality of
 - 4 fingers and producing a plurality of processing cycle boundary signals therefrom;
 - a register for storing the memory address in response to a processing cycle
 - 6 boundary signal; and
 - a sample processor for processing samples from the memory identified in
 - 8 accordance with the stored memory address.
5. The demodulator of claim 4, wherein the location of samples in the memory for
 - 2 processing in the sample processor is computed by subtracting the processing cycle length from the stored memory address.
6. The demodulator of claim 4, wherein the finger timing unit comprises a plurality
 - 2 of counters for producing the time reference for each of the plurality of fingers.

7. The demodulator of claim 4, wherein the finger timing unit comprises a single
2 counter and a plurality of masks for producing the time reference for each of the
plurality of fingers.
- 2 8. The demodulator of claim 4, wherein the processing cycle boundary is a symbol.
9. The demodulator of claim 4, wherein the sample processor comprises:
2 a pseudo-random noise (PN) generator for generating PN values; and
4 a despreader for despreading the samples with the PN values to produce
despread samples.
10. The demodulator of claim 9, further comprising a register for storing the time
2 reference corresponding to and in response to a processing cycle boundary signal.
11. The demodulator of claim 10, wherein the PN generator comprises a memory,
2 loaded with the PN sequence values, which is addressed in accordance with the stored
time reference.
12. The demodulator of claim 11, wherein the address is computed by subtracting
2 the processing cycle length from the stored time reference.
13. The demodulator of claim 11, wherein the address is computed by adding a base
2 station specific offset to the stored time reference and subtracting the processing cycle
length from the result thereof.
14. The demodulator of claim 9, wherein the sample processor further comprises:
2 a Walsh generator for generating Walsh chips; and
4 a Walsh decoder for discovering the despread samples to produce discovered
samples.
15. The demodulator of claim 14, wherein the sample processor further comprises
2 an accumulator for accumulating the discovered samples for one or more channels.

16. The demodulator of claim 4, further comprising an interrupt controller for
2 arbitrating between the plurality of processing cycle boundary signals.

17. The demodulator of claim 4, further comprising a DSP for processing and
2 combining the results of the sample processor.

18. The demodulator of claim 17, further comprising a direct memory access
2 (DMA) controller for delivering the output of the sample processor to the DSP.

19. A CDMA demodulator, comprising:
2 means for generating signals indicating cycle boundaries for a plurality of
fingers;
4 means for receiving and storing samples; and
means for processing symbols from the stored samples for the plurality of
6 fingers in response to the cycle boundary signals.

20. A CDMA system including a demodulator, comprising:
2 a finger timing unit for generating signals indicating cycle boundaries for a
plurality of fingers; and
4 an offline processing unit for receiving and storing samples and processing
symbols from the stored samples for the plurality of fingers in response to the cycle
6 boundary signals.

21. A method of CDMA demodulation, comprising:
2 storing received I and Q samples in a memory according to a memory address;
producing a time reference for a plurality of fingers;
4 generating interrupts on processing cycle boundaries according to the plurality
of time references; and
6 processing stored samples using an offline processing unit.

22. The method of claim 21, further comprising:
2 latching the memory address upon generating an interrupt; and
accessing the stored samples for processing using an address generated from the
4 latched memory address.
23. The method of claim 21, further comprising arbitrating between simultaneous
2 assertions of interrupts corresponding to one or more of the plurality of time references.
24. The method of claim 21, further comprising symbol demodulation and
2 combining of the results of the offline processing unit in a DSP.
25. The method of claim 24, further comprising:
2 performing time tracking for the plurality of time references in the DSP; and
updating the plurality of time references in accordance with the time tracking.
26. The method of claim 24, further comprising:
2 performing power control decoding in the DSP; and
modifying transmit power in accordance with the power control decoding.